AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

1. (Currently amended) A semiconductor device, comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate, said gate electrode and said insulating film defining at least one lightly doped first drain and source diffusion ~~layers~~ layer;

(d) at least one sidewall covering said gate electrode therewith; and

(e) at least one heavily doped second drain and source diffusion ~~layers~~ layer formed at a surface of said semiconductor substrate around said gate electrode, ~~and aligned with said at least one sidewall, with~~ wherein said at least one first drain and source diffusion ~~layers surrounding~~ layer contacts said at least one second drain and source diffusion ~~layers~~ layer on at least a bottom and a lateral side,

said at least one sidewall having connected thereto a sidewall offset extending outwardly of said gate electrode along ~~a horizontal~~ the surface of said semiconductor substrate in at least one of regions below which said at least one ~~of said~~ second drain and source diffusion ~~layers are~~ layer is to be formed, said sidewall offset having a lateral

dimension extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a thickness of said sidewall,

said at least one lightly doped first drain and source diffusion ~~layers~~ layer extending towards said gate electrode beyond an edge of said sidewall offset, and said at least one heavily doped second drain and source diffusion ~~layers~~ layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said ~~horizontal~~ surface of said semiconductor substrate;

wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.

2. (Original) The semiconductor device as set forth in claim 1, wherein said sidewall offset is formed along a surface of said semiconductor substrate in both regions below which said drain and source diffusion layers are to be formed.

3. (Original) The semiconductor device as set forth in claim 1, further comprising second diffusion layers formed below said drain and source diffusion layers and surrounding said drain and source diffusion layers.

4. (Original) The semiconductor device as set forth in claim 3, wherein said second diffusion layers have a lower impurity-concentration than that of said drain and source diffusion layers.

5. (Original) The semiconductor device as set forth in claim 1, further comprising a memory cell formed on said semiconductor substrate.

6. (Currently amended) A semiconductor device, comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate, said gate electrode and said insulating film defining at least one lightly doped first drain and source diffusion ~~layers~~ layer;

(d) at least one sidewall covering said gate electrode therewith;

(e) at least one heavily doped second drain and source diffusion ~~layers~~ layer formed at a surface of said semiconductor substrate around said gate electrode, ~~and aligned with said at least one sidewall, with~~ wherein said at least one first drain and source diffusion ~~layers surrounding~~ layer contacts said at least one second drain and source diffusion ~~layers~~ layer on at least a bottom and a lateral side,

said at least one sidewall having connected thereto a sidewall offset extending outwardly of said gate electrode along ~~a horizontal~~ the surface of said semiconductor substrate in at least one of regions below which said at least one ~~of said~~ second drain and source diffusion ~~layers are~~ layer is formed, said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a thickness of said sidewall; and

(f) low-resistive wiring layers formed at surfaces of said drain and source diffusion layers, said low-resistive wiring layers being located outwardly beyond a peripheral edge of at least one of said sidewall and said sidewall offset in said at least one of said drain and source diffusion layers,

said at least one lightly doped first drain and source diffusion ~~layers~~ layer extending towards said gate electrode beyond an edge of said sidewall offset, and said at least one heavily doped second drain and source diffusion ~~layers~~ layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said ~~horizontal~~ surface of said semiconductor substrate;

wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.

7. (Original) The semiconductor device as set forth in claim 6, wherein said low-resistive wiring layers are composed of TiSi.

8. (Original) The semiconductor device as set forth in claim 6, wherein said sidewall offset is formed along a surface of said semiconductor substrate in both regions below which said drain and source diffusion layers are to be formed.

9. (Original) The semiconductor device as set forth in claim 6, further comprising second diffusion layers formed below said drain and source diffusion layers and surrounding said drain and source diffusion layers.

10. (Original) The semiconductor device as set forth in claim 9, wherein said second diffusion layers have a lower impurity-concentration than that of said drain and source diffusion layers.

11. (Original) The semiconductor device as set forth in claim 6, further comprising a memory cell formed on said semiconductor substrate.

Claims 12-19 (Cancelled)

20. (Previously presented) The semiconductor device of Claim 1, wherein said sidewall offset extends in only one direction towards said source and drain diffusion layers.

21. (Previously presented) The semiconductor device of Claim 1, wherein said sidewall entirely covers said gate electrode.

22. (Previously presented) The semiconductor device of Claim 6, wherein said sidewall offset extends in only one direction from said gate electrode towards said source and drain diffusion layers.

23. (Previously presented) The semiconductor device of Claim 6, wherein said sidewall entirely covers said gate electrode.